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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,136	11/03/2003	Tomio Matsuzaki	03663/LH	3722

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EXAMINER

LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/700,136	MATSUZAKI ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-16 and 36-53 is/are pending in the application.
- 4a) Of the above claim(s) 5-11 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,4,12-16 and 36-53 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>1/17/06</u> . | 6) <input type="checkbox"/> Other: _____ |

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1. Applicant is advised that should claim 13 be found allowable, claim 48 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

2. Applicant is advised that should claim 16 be found allowable, claim 51 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

3. Claims 40-45 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses an upper insulating film formed between the insulating film and the encapsulating film, said upper insulating film having a hole formed in a portion corresponding to each said bump electrode as claimed in claim 40.

The specification never discloses each said bump electrode protrudes from an upper surface of the encapsulating film as claimed in claim 43.

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The specification never discloses each said bump electrode comprises a lower bump electrode and an upper bump electrode formed on the lower bump electrode as claimed in claim 44.

The specification never discloses the lower bump electrode protrudes from an upper surface of the encapsulating film as claimed in claim 45.

4. Claims 3, 36-47, 49, 50 and 53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3, lines 3-5, claim 36, lines 22-24, the phrase "a space is provided between each said at least one interconnection and the side surfaces of the recess in which the interconnection is provided" is vague and indefinite. Fig. 1 discloses a space is provided between each said at least one interconnection [8] and a corresponding side surface of the recess [7] in which the interconnection is provided. Therefore, it is believed that the phrase should rewrite as "a space is provided between each said at least one interconnection and a corresponding side surface of the recess in which the interconnection is provided".

Claim 36, line 21, the phrase "said recess" is unclear whether it is being referred to "said at least one recess" in lines 8-9 of claim 36.

Claim 37, lines 20-22, the phrase "a space is provided between each of the interconnections and the side surfaces of the recess in which the interconnection is provided" is vague and indefinite. Fig. 1 discloses a space is provided between each of the interconnections [8] and a corresponding side surface of the recess [7] in which the

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interconnection is provided. Therefore, the phrase should rewrite as "a space is provided between each of the interconnections and a corresponding side surface of the recess in which the interconnection is provided".

Claim 53, lines 2-5, the phrase "a lower layer and an upper layer formed on an entire upper surface of the lower layer so as not to laterally extend from the upper surface of the lower layer" is vague and indefinite. Fig. 1 discloses a lower layer [8a] and an upper layer [8b] formed on an entire upper surface of the lower layer [8a] so as to laterally extend on the upper surface of the lower layer. Therefore, it is believed that the phrase should rewrite as "a lower layer and an upper layer formed on an entire upper surface of the lower layer so as to laterally extend on the upper surface of the lower layer".

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4, 13, 48, 52 and 53 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sakamoto et al.

In regards to claim 1, Sakamoto et al. show all the elements of the claimed invention in figs. 10A and 10B. It is a semiconductor device, comprising: a semiconductor substrate [12] having a plurality of connecting pads (a lower portion of layer SD) on one surface; an insulating film (the lower portion of the under-fill material AF and a lower portion of layer [14]) (paragraphs [0052] and [0053]) which is formed of a single layer and covers said one surface of the semiconductor substrate, and which includes: (i) a

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plurality of holes (the area where the upper portion of layer SD is formed) extending through the insulating film, each of the holes corresponding to one of the connecting pads, and (ii) at least one recess (the area adjacent the lower portion of layer [14] that has a flat bottom surface (near DM)) extending partially through the insulating film such that a bottom surface of the recess is depressed with respect to an upper surface of the insulating film (the top surface of the lower portion of layer [14]) in a direction of thickness of the insulating film; each said recess including a first portion (an inner portion of the recess) through which one of the holes extends and which surrounds a periphery of the one of the holes and a second portion (an outer portion of the recess) which extends outwardly from the first portion; and at least one interconnection (layer [11A] and the upper portion of SD formed between the lower portion of SD and [23]) formed on the bottom surface of a corresponding said at least one recess to extend along the bottom surface, over the first portion and the second portion of the recess, each said at least one interconnection being directly contacted to a corresponding one of the connecting pads through a corresponding one of the holes in the insulating film, and each said at least one interconnection being formed of a same material along an entire length thereof (e.g. an entire length of layer [11A] is formed of Cu (paragraph [0054])).

In regards to claim 4, Sakamoto et al. further disclose the at least one interconnection comprises a connecting pad portion, and wherein the semiconductor device further comprises: a bump electrode (an upper portion of layer [23]) formed on the connecting pad portion, and an encapsulating film (an upper portion of the under-fill

material AF and an upper portion of layer [14]) formed around the bump electrode and on the insulating film and the at least one interconnection.

In regards to claims 13, 48, Sakamoto et al. further disclose the recess in the insulating film has a depth which is not less than a thickness of the interconnection.

In regards to claim 53, Sakamoto et al. further disclose the at least one interconnection comprises a lower layer (the upper portion of layer SD) and an upper layer [11A] formed on an entire upper surface of the lower layer so as to laterally extend on the upper surface of the lower layer.

In regards to claim 52, Sakamoto et al. show all the elements of the claimed invention in figs. 10A and 10B. It is a semiconductor device, comprising: a semiconductor substrate [12] having a plurality of connecting pads (the lower portions of layers SD) on one surface; a protective film (the under-fill material AF and the layer [14]) (paragraphs [0052] and [0053]) formed of a single layer, said protective film including: (i) a plurality of holes extending completely through the protective film, each of the holes corresponding to one of the connecting pads, and (ii) a plurality of recesses (the area adjacent the layer [14] that has a flat bottom surface (near DM)) extending partially through the protective film, each of said recesses having a recessed surface that is lower than an upper surface of the protective film in a thickness direction of the protective film, and each of said recesses including a first portion (an inner portion of the recess) through which one of the holes extends and which surrounds a periphery of the one of the holes and a second portion (an outer portion of the recess) which extends outwardly from the first portion; and a plurality of interconnections (layers [11A] and the

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upper portion of SD formed between the lower portions of SD and [23]) which are respectively connected to the connecting pads through the holes in the protective film, and which are provided on the recessed surfaces of the protective film to extend along the recessed surfaces over the first and second portions of the recessed surfaces, and each of which is formed of a same material along an entire length thereof (e.g. an entire length of layer [11A] is formed of Cu (paragraph [0054])).

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 12, 14-16 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al.

In regards to claim 12, Sakamoto et al. differ from the claimed invention by not showing the insulating film is made of an organic resin.

It would have been obvious for the insulating film is made of an organic resin because it is a widely used material to protect the chip from the external environment.

In regards to claim 14, Sakamoto et al. differ from the claimed invention by not showing the insulating film has a thickness of 10 to 30 μm .

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the insulating film has a thickness of 10 to 30 μm , since it has been held that where the general conditions of a claim are disclosed in the prior art,

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discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claim 15, Sakamoto et al. differ from the claimed invention by not showing the recess has a depth of 5 to 15 μm .

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the recess has a depth of 5 to 15 μm , since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claims 16, 51, Sakamoto et al. differ from the claimed invention by not showing a distance between a bottom surface of the insulating film and the bottom surface of the recess is not less than 1 μm .

It would have been obvious to one having ordinary skill in the art at the time the invention was made for a distance between a bottom surface of the insulating film and the bottom surface of the recess is not less than 1 μm , since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

9. Applicant's arguments filed 3/28/06 have been fully considered but they are not persuasive.

It is urged, in pages 18 and 19 of the remarks, that Sakamoto et al. clearly does not disclose, teach or suggest a recess in an insulating or protective film that has a first portion in which a hole (corresponding to a connecting pad) is formed and which

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surrounds the hole, and a second portion that extends outwardly from the first portion.

However, the area adjacent to the lower portion of layer [14] that has a flat bottom surface (near DM) is considered as the recess that including a first portion (an inner portion of the recess) through which one of the holes extends and which surrounds a periphery of the one of the holes and a second portion (an outer portion of the recess) which extends outwardly from the first portion. Then the interconnection (the layer [11A]) extends along the bottom surface of the recess along both the first and second portions.

10. Claims 36 and 37 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

11. Claim 3 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sl
June 9, 2006

Steven Lake
Primary Examiner
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